WHAT IS CLAIMED IS:

1. A high-voltage MOS transistor wherein a resistance value of a source region is set independently of a resistance value of a drain region in such a manner as to increase a sustaining breakdown voltage of the transistor.

2. The transistor of Claim 1, wherein a resistance value of a source offset region is set independently of a resistance value of a drain offset region in such a manner as to increase the sustaining breakdown voltage of the transistor.

3. A high-voltage MOS transistor comprising:

a drain offset region; and

a source offset region, which is asymmetrical to the drain offset region,

whereby the transistor has a high sustaining breakdown voltage.

4. The transistor of Claim 3, wherein a [size] of the source offset region is not equal to a [size] of the drain offset region such that the transistor has the high sustaining breakdown voltage.

5. The transistor of Claim 3, wherein a dopant concentration of the source offset region is not equal to a dopant

concentration of the drain offset region such that the transistor has the high sustaining breakdown voltage.

6. A high-voltage MOS transistor comprising:

a drain offset region; and

a source offset region, which has a dopant concentration different from that of the drain offset region,

whereby the transistor has a high sustaining breakdown voltage.

fig. 4

7. The transistor of Claim 1, wherein the resistance value of the source region is set higher than that of the drain region such that a substrate voltage VW minus [a forward biased breakdown voltage] of silicon does not exceed a source voltage VS easily.

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8. A method for fabricating a high-voltage MOS transistor, comprising the steps of:

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defining a resist pattern that makes a size of a source offset region greater than a size of a drain offset region; and

forming the source and drain offset regions using the resist pattern to increase a sustaining breakdown voltage of the transistor.

9. A method for fabricating a high-voltage MOS transistor, comprising the steps of:

forming a drain offset region; and

forming a source offset region by implanting dopant ions at such a level as setting a dopant concentration of the source offset region independently of a dopant concentration of the drain offset region to increase a sustaining breakdown voltage of the transistor.

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10. The method of Claim 9, wherein the dopant concentration of the source offset region is set lower than that of the drain offset region.

11. A method for fabricating a high-voltage MOS transistor, which will be formed along with a low-voltage MOS transistor on the same chip, the method comprising the steps of:

shifting a photomask for forming a well for the low-voltage MOS transistor and source and drain well offset regions for the high-voltage MOS transistor to such a position as making a size of a region overlapping between the source well offset region and a source offset region smaller than that of a region overlapping between the drain well offset region and a drain offset region; and

forming the source and drain well offset regions for the high-voltage MOS transistor using the photomask to increase a

sustaining breakdown voltage of the high-voltage MOS transistor.